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TITLE: Deposition film surface treatment method used during semiconductor device manufacture, involves performing plasma etching process using mixed gas of chlorine and oxygen, hydrogen bromide

PRIORITY-DATA: 2000JP-0219562 (July 19, 2000)

Masamichi et al.

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2002043284 A	February 8, 2002		007	H01L021/3065

INT-CL (IPC): H01 L 21/28; H01 L 21/3065; H01 L 21/3205; H01 L 21/3213; H01 L 29/43

ABSTRACTED-PUB-NO: JP2002043284A
BASIC-ABSTRACT:

NOVELTY - A silicon deposition film is processed using hydrogen bromide (HBr), and the mixture of chlorine gas and oxygen gas. The mixing rate of oxygen and chlorine is 0.5-30%.

USE - For performing etching process of silicon deposition film on surface of semiconductor element used during semiconductor device manufacture.

ADVANTAGE - The side wall of the n-type gate electrode pattern is protected during the plasma etching process, hence surface treatment is performed with high accuracy.

DESCRIPTION OF DRAWING(S) - The figure explains a sectional view of the plasma etching process.

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PATENT ABSTRACTS OF JAPAN

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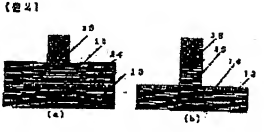
(54) STACKED FILM SURFACE TREATING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a stacked film surface treating method capable of treating a stacked silicon film with anisotropy and high precision when treating it with a plasma etching device.
SOLUTION: Treatment is divided into several steps until exposing a gate oxide film 14 and for removing residue on the side wall of a gate electrode polycrystal silicon part 15 and the film 14. Plasma etching using gaseous hydrogen bromide (HBr) or mixed gas containing hydrogen bromide (HBr) is performed in at least one step in a former half and plasma etching using mixed gas of chloride (Cl2) and oxide (O2) is performed in at least one step in a latter half.



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21/28			301A	5F004
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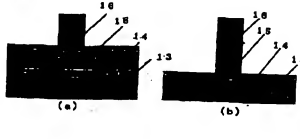
(54)【発明の名称】　堆積膜表面処理方法

(57)【要約】　（修正有）
【課題】　プラズマエッチング装置によって処理加工する際に、シリコン堆積膜を、異方性で、高い加工精度によって処理加工することが可能な堆積膜表面処理方法を提供する。
【解決手段】　加工処理をゲート酸化膜１４を露出するまでと、ゲート電極多結晶シリコン部１５の側壁及びゲート酸化膜１４上の残渣を除去するための複数のステップに分けて行うようにし、前半の少なくとも１つのステップにおいて臭化水素（ＨＢｒ）ガスまたは臭化水素（ＨＢｒ）を含有する混合ガスを用いたプラズマエッチング処理を行い、後半の少なくとも１つのステップにおいて塩素（Cl_2）と酸素（O_2）の混合ガスを用いてプラズマエッチング処理を行う。

【図２】



【特許請求の範囲】

【請求項１】　シリコン堆積膜をプラズマエッチング装置によって処理加工する堆積膜表面処理方法であって、前記加工処理を複数のステップに分けて行うようにし、前記複数のステップの中の前半の少なくとも１つのステップにおいて臭化水素（ＨＢｒ）ガスまたは臭化水素（ＨＢｒ）を含有する混合ガスを用いたプラズマエッチング処理を行い、かつ、前記複数のステップの中の後半の少なくとも１つのステップにおいて塩素（Ｃｌ２）と酸素（Ｏ２）の混合ガスを用いてプラズマエッチング処理を行うことを特徴とする堆積膜表面処理方法。

【請求項２】　前記シリコン堆積膜は、導電性の異なる膜を共有するデュアルゲート膜構造のものであることを特徴とする請求項１記載の堆積膜表面処理方法。

【請求項３】　前記シリコン堆積膜は、高融点金属または高融点金属のシリサイドを有するものであることを特徴とする請求項１または２のいずれかに記載の堆積膜表面処理方法。

【請求項４】　前記塩素（Ｃｌ２）と酸素（Ｏ２）の混合ガスは、酸素（Ｏ２）の混合率が０．５％乃至３０％の範囲内であることを特徴とする請求項１乃至３のいずれかに記載の堆積膜表面処理方法。

【請求項５】　前記シリコン堆積膜は、加工処理する際に用いるマスクの材料として、炭素を主成分とするもの、窒化シリコンからなるもの、酸化シリコンからなるもの、あるいはこれらを多層にしたものを用いていることを特徴とする請求項１乃至４のいずれかに記載の堆積膜表面処理方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、堆積膜表面処理方法に係わり、特に、プラズマ発生装置を用いて半導体素子表面のシリコン堆積膜のエッチング処理を行うのに適した堆積膜表面処理方法に関する。

【０００２】

【従来の技術】従来、半導体装置の製造工程においては、半導体素子表面の加工処理、例えば半導体素子の表面に堆積したシリコン堆積膜をエッチング処理する処理工程を含んでいる。そして、このシリコン堆積膜のエッチング処理には、通常、プラズマエッチング装置を用いているもので、エッチング処理すべき半導体素子をプラズマエッチング装置内に入れ、プラズマ雰囲気中で所要のエッチング処理を行っているものである。

【０００３】この場合、半導体素子表面のエッチング処理に使用されるプラズマエッチング装置には、主として高い加工精度を得るものとして、米国特許第４，４９０，２０９号明細書に開示されたプラズマエッチング装置が知られている。ここに開示されたプラズマエッチング装置は、プラズマとなるガスに臭化水素（ＨＢｒ）を添加したもので、臭化水素（ＨＢｒ）を添加したことにより、被加工物質であるシリコン（Ｓｉ）膜を異方性にエッチング処理することができるものである。

【０００４】ところで、近年、各種の情報内容が高密度化したのに伴い、このような高密度情報を処理する半導体装置の構成も微細構造のものになっており、半導体装置内に形成される大規模集積回路（ＬＳＩ）についても、配線や電極を加工する際に高い加工精度が要求される。

【０００５】このような微細構造の半導体装置において、例えば２５６ＭＢｉｔを超えるメモリ素子を構成する場合には、メモリ素子の構成要素となる各ＭＯＳトランジスタのゲート酸化膜の厚さを６ｎｍ以下に形成する必要がある。そして、このようなＭＯＳトランジスタは、異方性と下地のゲート酸化膜との選択比がトレードオフの関係になるため、エッチング処理によって得ることが極めて難しくなってきている。

【０００６】これと同時に、近年、半導体装置においては、高速化及び低消費電力化が要望されるに伴い、ｎＭＯＳトランジスタ等のｎＭＯＳ素子とｐＭＯＳトランジスタ等のｐＭＯＳ素子とを組み合わせたＣＭＯＳ素子が多く用いられるようになっている。このＣＭＯＳ素子は、ｐＭＯＳ側のゲート電極領域となる多結晶シリコン内にｐ型不純物をドープし、ｎＭＯＳ側をゲート電極領域となる多結晶シリコン内にｎ型不純物をドープしたいわゆるデュアルゲート構造を備えるものである。

【０００７】

【発明が解決しようとする課題】ＣＭＯＳ素子のように、導電性を異にするゲート電極、すなわちｐ型ゲート電極及びｎ型ゲート電極が混在した相補ゲート電極を備える場合、その相補ゲート電極部分をエッチングによって形成する際には、単一導電性のゲート電極部分をエッチングによってを形成する場合に比べて、以下に述べるように、加工上種々の制約が生じることになる。

【０００８】すなわち、相補ゲート電極を形成する場合、例えばリソグラフィ工程を増加して、ｐ型ゲート電極領域とｎ型ゲート電極領域とを個別のエッチング処理によって形成すると、その分処理工程が増えることになり、全体の製造コストが増大するようになる。このため、ｐ型ゲート電極領域とｎ型ゲート電極領域とは、どうしても同時エッチング処理によって形成する必要がある。これに対し、ｐ型ゲート電極領域とｎ型ゲート電極領域とを同時エッチング処理によって形成すると、ｎ型ゲート電極となるｎ型多結晶シリコン部分のエッチング速度が、ｐ型ゲート電極となるｐ型多結晶シリコン部分のエッチング速度に比べて大きいため、ｎ型ゲート電極領域近傍の下地ゲート酸化膜が早く露出するようになり、露出したゲート酸化膜がエッチング処理され、その処理部分のゲート酸化膜が薄くなったり、その処理部分のゲート酸化膜に突き抜けが生じたりする場合があり、エッチング処理されたｎ型ゲート電極にサイドエッチが

発生したりする場合もある。

【０００９】図３（ａ）乃至（ｄ）は、ｎ型多結晶シリコン部分を既知の表面処理方法によってプラズマエッチング加工し、ｎ型ゲート電極パターンを得る際に、ｎ型ゲート電極パターンの変化状態を示す断面図であって、（ａ）は加工前の状態、（ｂ）乃至（ｄ）は加工後の種々の状態であり、その中で、（ｂ）はゲート酸化膜上にエッチング残渣がある状態、（ｃ）はｎ型ゲート電極パターンにサイドエッチが入った状態、（ｄ）はゲート酸化膜に突き抜けが生じた状態を示すものである。

【００１０】図３（ａ）乃至（ｄ）において、３１はシリコン基板、３２はゲート酸化膜、３３はｎ型不純物をドープしたｎ型多結晶シリコン部、３４はマスク、３５はエッチング残渣、３６はサイドエッチ、３７はゲート酸化膜突き抜け部である。

【００１１】まず、プラズマエッチング加工前の状態は、図３（ａ）に示されるように、シリコン基板３１の一面にゲート酸化膜３２が形成され、ゲート酸化膜３２上にｎ型多結晶シリコン部３３が設けられている。また、ｎ型多結晶シリコン部３３上のｎ型ゲート電極パターン形成部にマスク３４が装着されている。

【００１２】この場合、既知の表面処理方法においては、プラズマエッチング加工を行う際に、臭化水素（ＨＢｒ）、塩素（Cl_2）及び酸素（O_2）の混合ガスを用い、エッチング条件として、エッチングトータルガス流量が５０乃至３００ｍＬ／ｍｉｎ、処理圧力が０．２乃至４．０Ｐａ、マイクロ波電力が４００乃至１０００Ｗで、その混合ガスのガス混合比及び高周波バイアスの電力値をそれぞれ選ぶことにより、好適なプラズマエッチング加工が行われるように設定している。

【００１３】しかるに、このようなエッチング条件を設定したとしても、以下に述べるような種々の加工状態になることが多い。

【００１４】その第１は、図３（ｂ）に示されるように、ゲート酸化膜３２上にエッチング残渣がある加工状態で、マスク３４の装着領域に該当するｎ型ゲート電極パターン（ｎ型多結晶シリコン部３３）を除いた大部分のｎ型多結晶シリコン部３３がエッチング除去されているものの、ゲート酸化膜３２上に僅かながらエッチング除去されないｎ型多結晶シリコン部３３のエッチング残渣３５が残留しているものである。

【００１５】その第２は、図３（ｃ）に示されるように、加工されたｎ型ゲート電極パターンにサイドエッチ３６が入った加工状態で、マスク３４の装着領域に該当するｎ型ゲート電極パターン（ｎ型多結晶シリコン部３３）を除いた全てのｎ型多結晶シリコン部３３がエッチング除去されているものの、ｎ型ゲート電極パターンの側壁の保護が不十分であるため、ゲート酸化膜３２との接合領域に近いｎ型ゲート電極パターンがエッチング除去され、サイドエッチ３６が形成される。

【００１６】その第３は、図３（ｄ）に示されるように、ゲート酸化膜３２に突き抜け部３７が形成された加工状態で、マスク３４の装着領域に該当するｎ型ゲート電極パターン（ｎ型多結晶シリコン部３３）を除いた全てのｎ型多結晶シリコン部３３がエッチング除去されているだけでなく、ｎ型ゲート電極パターン周辺のゲート酸化膜３２の露出が早かったため、露出したゲート酸化膜３２が順次エッチング除去されてしまい、ゲート酸化膜３２に突き抜け部３７が形成される。

【００１７】このように、既知の表面処理方法は、プラズマエッチング加工を行うときのエッチング条件を厳密に設定しない限り、所要の高い加工精度による処理加工を行うことが難しいものであった。

【００１８】そこで、ゲート電極パターンのエッチングにおいて、下地のゲート酸化膜が露出した時点で、エッチング時のプロセス、例えば臭化水素（ＨＢｒ）と塩素（Cl_2）と酸素（O_2）の混合ガスに代えて、臭化水素（ＨＢｒ）と酸素（O_2）の混合ガスを用いてオーバーエッチングすることにより残渣やサイドエッチやゲート酸化膜の突き抜けを防止する手段が講じられている。この場合、例えば混合ガスの流量を１００／５（ｍｌ／ｍｉｎ）、処理圧力を１．２Ｐａ以上、マイクロ波電力を０．４乃至１．０ＫＷ、バイアス電力を３０乃至４０Ｗとしてオーバーエッチング処理を実行する。

【００１９】しかしながら、この手段は、臭化水素（ＨＢｒ）と酸素（O_2）の混合ガスによる処理の処理圧力が高く、処理室内へのデポ物の付着が増大するという問題があった。

【００２０】本発明は、このような技術的背景に鑑みてなされたもので、その目的は、シリコン堆積膜をプラズマ発生装置によって処理加工する際に、シリコン堆積膜を、異方性で、高い加工精度によって処理加工することを可能にした堆積膜表面処理方法を提供することにある。

【００２１】

【課題を解決するための手段】前記目的を達成するために、本発明による堆積膜表面処理方法は、シリコン堆積膜をプラズマエッチング装置によって処理加工するものであって、加工処理を複数のステップに分けて行うようにし、複数のステップの中の前半の少なくとも１つのステップにおいて臭化水素（ＨＢｒ）ガスまたは臭化水素（ＨＢｒ）を含有する混合ガスを用いたプラズマエッチング処理を行い、かつ、複数のステップの中の後半の少なくとも１つのステップにおいて塩素（Cl_2）と酸素（O_2）の混合ガスを用いてプラズマエッチング処理を行う手段を具備する。

【００２２】前記手段によれば、シリコン堆積膜の下地のゲート酸化膜が露出するまでは、臭化水素（ＨＢｒ）ガスまたは臭化水素（ＨＢｒ）を含有する混合ガスを用いた第１のプラズマエッチング処理を行い、この第１の

プラズマエッチング処理によってエッチング残渣がなく、かつ、ゲート酸化膜に突き抜け部が形成されない状態のｎ型ゲート電極パターンを形成することができ、また、シリコン堆積膜の下地のゲート酸化膜が露出した後は、塩素（Cl_2）と酸素（O_2）の混合ガスを用いた第２のプラズマエッチング処理を行い、この第２のプラズマエッチング処理によって得られた多くの反応生成物がｎ型ゲート電極パターンの側壁に吸着されるので、ｎ型ゲート電極パターンの側壁が第２のプラズマエッチング処理に対して保護され、サイドエッチが発生しないｎ型ゲート電極パターンを形成することができる。

【００２３】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照して説明する。

【００２４】図１は、本発明による堆積膜表面処理方法を実施するのに用いられるプラズマエッチング装置の構成の概要を示す断面図である。

【００２５】図１に示されるように、プラズマエッチング装置は、真空容器１と、真空容器１の一端側開口部を封止するマイクロ波導入窓２と、真空容器１の他端側に配置されたガス排気口３と、真空容器１の外周面に沿って設置される電磁石４と、真空容器１の内部に配置され、表面に絶縁膜６が形成された試料台５と、試料台５上に載置された試料となる半導体素子基板７と、一端がマイクロ波導入窓２で終端しているマイクロ波導入部８と、マイクロ波導入部８の他端に接続されたマイクロ波発生源９と、試料台５に導電接続された高周波（ＲＦ）バイアス電源１０及び可変直流電源１１と、真空容器１内にガスを導入するガス導入部１２とからなっている。また、真空容器１の内部にプラズマ領域Ｐが形成される。

【００２６】この場合、マイクロ波導入窓２は、材質が石英、セラミック等のマイクロ波（電磁波）の透過物質からなっている。マイクロ波発生源９から出力されたマイクロ波は、マイクロ波導入部８を通り、マイクロ波導入窓２を透過して真空容器１の内部に導入される。ガス導入部１２は、ハロゲンガス等のエッチングガスを真空容器１の内部に導入する。真空容器１の内部では、このエッチングガスにマイクロ波が作用し、エッチングガスによるプラズマ領域Ｐが形成される。電磁石４は、真空容器１内に磁場を発生させるものである。電磁石４が発生する真空容器１内の磁場強度は、真空容器１内に導入されたマイクロ波周波数と共鳴を起すような値に設定されており、例えばマイクロ波周波数が２．４５ＧＨｚであったとき、磁場強度が０．０８７５Ｔ程度になるように選択される。このような磁場強度に選択されることにより、プラズマ領域Ｐ中の電子のサイクロトロン運動がマイクロ波周波数と共鳴し、マイクロ波エネルギーが効率よくプラズマＰに供給され、高密度のプラズマＰが形成される。

【００２７】半導体素子基板７は、シリコン堆積膜がエッチング処理されるもので、試料台５の上に載置される。この試料台５には、表面にセラミックあるいはポリマー膜からなる絶縁膜６が形成されている。高周波バイアス電源１０は、試料台５に高周波バイアスを供給し、半導体素子基板７に入射するイオンを加速する。また、可変直流電源１１は、直流電圧を試料台５に与え、そのとき発生する静電力によって半導体素子基板７を試料台５の上に保持させるものである。

【００２８】ここで、図１に図示のプラズマエッチング装置を用い、半導体素子基板７のシリコン堆積膜をエッチング加工する場合の動作について説明する。この場合、シリコン堆積膜は、多結晶シリコン内にｎ型不純物をドープして形成したｎ型多結晶シリコンであって、このｎ型多結晶シリコンをエッチング加工し、ｎ型ゲート電極パターンを得るものである。

【００２９】図２（ａ）、（ｂ）は、図１に図示されたプラズマエッチング装置を用い、半導体素子基板７のシリコン堆積膜をプラズマエッチング加工してｎ型ゲート電極パターンを得る際に、ｎ型ゲート電極パターンの変化状態を示す断面図であって、（ａ）は加工前の状態、（ｂ）は加工後の状態である。

【００３０】図２（ａ）、（ｂ）において、１３はシリコン基板、１４はゲート酸化膜、１５はｎ型不純物をドープしたｎ型多結晶シリコン部及びｐ型ゲート電極パターン、１６はマスクである。

【００３１】そして、プラズマエッチング加工前の状態は、図２（ａ）に示されるように、シリコン基板１３の一面にゲート酸化膜１４が形成され、ゲート酸化膜１４上にｎ型多結晶シリコン部１５が設けられている。また、ｎ型多結晶シリコン部１５上のｎ型ゲート電極パターン形成部にマスク１６が装着されているもので、図３（ａ）に図示された構成と同じ構成のものである。

【００３２】ところで、本発明による堆積膜表面処理方法においては、半導体素子基板７のシリコン堆積膜に対するプラズマエッチング加工を行う際に、複数のステップを経て所要のプラズマエッチング処理を行うもので、プラズマエッチング加工によりゲート酸化膜１４が露出するまでの第１のプラズマエッチング処理と、ゲート酸化膜１４が露出した後の第２のプラズマエッチング処理とに分かれている。

【００３３】この場合、第１のプラズマエッチング処理は、臭化水素（ＨＢｒ）ガス、または、臭化水素（ＨＢｒ）を含有する混合ガスを用いたプラズマエッチング処理であって、この場合、臭化水素（ＨＢｒ）、塩素（Cl_2）及び酸素（O_2）の混合ガスを用い、例えば流量を７０／３０／３～５（ｍｌ／ｍｉｎ）、処理圧力を０．２～１．０Ｐａ、マイクロ波電力を０．４～１．０ＫＷ、バイアス電力を３０Ｗとし、ゲート酸化膜１４の大部分が露出するまでこの第１のプラズマエッチング処

理を実行する。第１のプラズマエッチング処理を行った場合、ｎ型多結晶シリコン部１５のマスク１６が装着されていない領域は、臭素（Ｂｒ）、塩素（Ｃｌ２）等のハロゲン原子イオン及びラジカルがｎ型多結晶シリコン１５と反応してエッチング処理が進行し、その処理の結果、ｎ型ゲート電極パターン１５が形成される。第１のプラズマエッチング処理時に生成された反応生成物の大部分は排気されるが、反応生成物の一部はｎ型ゲート電極パターン１５の側壁に吸着する。なお、第１のプラズマエッチング処理においては、臭化水素（ＨＢｒ）に含まれる水素（Ｈ２）原子がｎ型ゲート電極パターン１５の側壁に吸着する反応生成物の吸着量を抑制する。このため、臭化水素（ＨＢｒ）ガスの混合率を高くした場合は、垂直方法のエッチング加工度が向上するものの、ｎ型ゲート電極パターン１５にサイドエッチが生じることがあるので、臭化水素（ＨＢｒ）ガスの混合率を適宜選択することが好ましい場合がある。

【００３４】また、第２のプラズマエッチング処理は、塩素（Ｃｌ２）及び酸素（Ｏ２）の混合ガスを用いたプラズマエッチング処理であって、例えば流量を９０／１０（ｍｌ／ｍｉｎ）、処理圧力を０．３～１．０Ｐａ、マイクロ波電力を０．４～１．０ＫＷ、バイアス波電力を１５Ｗとし、ゲート酸化膜１４上にエッチング残渣がなくなるまでこの第２のプラズマエッチング処理を実行する。第２のプラズマエッチング処理を行った場合、生成された反応生成物の多くがｎ型ゲート電極パターン１５の側壁に吸着するので、ｎ型ゲート電極パターン１５の加工寸法が僅かに大きくなるものの、ｎ型ゲート電極パターン１５にサイドエッチが生じることがなく、しかも、エッチング残渣の除去の際に下地のゲート酸化膜１４に突き抜け部を形成することがなく、異方性の加工が可能になる。

【００３５】その結果、プラズマエッチング加工後の状態は、図２（ｂ）に示されるように、下地のゲート酸化膜１４上にエッチング残渣がなく、ｎ型ゲート電極パターン１５にサイドエッチが生じておらず、下地のゲート酸化膜１４に突き抜け部も形成されていない状態になり、かつ、異方性の加工が可能となるものである。

【００３６】この第２のプラズマエッチング処理に用いる塩素（Ｃｌ２）及び酸素（Ｏ２）の混合ガスは、酸素（Ｏ２）の混合率が０．５％乃至３０％の範囲内に選択することが好ましい。

【００３７】一方、マスク１６の構成材料は、炭素を主成分とするもの、または、炭素を含まないもののいずれを用いても同じマスク機能を発揮することができるが、窒化シリコンや酸化シリコン等からなる炭素を含まないものを用いた場合、下地のゲート酸化膜１４との選択性が高くなる。

【００３８】なお、前記の説明においては、本発明による堆積膜表面処理方法でプラズマエッチング処理する半導体素子基板７のシリコン堆積膜がｎ型多結晶シリコン部１５の単一層である例であったが、本発明による堆積膜表面処理方法の対象となるシリコン堆積膜は、ｎ型多結晶シリコン部１５の単一層である例に限られず、堆積膜がｐ型不純物をドープしたｐ型ドープ領域とｎ型不純物をドープしたｎ型ドープ領域とを共有するとデュアルゲート膜構造であるもの、シリコン膜上に、タングステン（Ｗ）、ニッケル（Ｎｉ）、コバルト（Ｃｏ）、チタン（Ｔｉ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）等の高融点金属層や、拡散を防ぐバリア膜としてこれらの金属の窒化物を含む層を積層したもの、あるいは、これらの金属のシリサイドを有するシリコン膜であっても、同じようにプラズマエッチング処理を行うことが可能である。

【００３９】また、本発明による堆積膜表面処理方法は、プラズマ生成方法に係わりなく、同様の機能を達成させることができる。

【００４０】以上の実施の形態によれば、従来行われていた処理圧力の高い臭化水素（ＨＢｒ）と酸素（Ｏ２）の混合ガスによるオーバーエッチング処理に代えて、処理圧力の低い塩素（Ｃｌ２）と酸素（Ｏ２）の混合ガスによるオーバーエッチング処理を実行することにより、残渣、サイドエッチ、下地のゲート酸化膜の突き抜けもなく、異方性で高い加工精度のエッチング加工処理ができるとともに、処理室へのデポ物の付着を少なくすることができる。

【００４１】

【発明の効果】以上のように、本発明の堆積膜表面処理方法によれば、シリコン堆積膜の下地のゲート酸化膜が露出するまでは、臭化水素（ＨＢｒ）ガスまたは臭化水素（ＨＢｒ）を含有する混合ガスを用いた第１のプラズマエッチング処理を行い、この第１のプラズマエッチング処理によってエッチング残渣がなく、かつ、ゲート酸化膜に突き抜け部が形成されない状態のｎ型ゲート電極パターンを形成することができ、また、シリコン堆積膜の下地のゲート酸化膜が露出した後は、塩素（Ｃｌ２）と酸素（Ｏ２）の混合ガスを用いた第２のプラズマエッチング処理を行い、この第２のプラズマエッチング処理によって得られた多くの反応生成物がｎ型ゲート電極パターンの側壁に吸着されるので、ｎ型ゲート電極パターンの側壁が第２のプラズマエッチング処理に対して保護され、サイドエッチが発生しないｎ型ゲート電極パターンを形成することができるという効果がある。

【図面の簡単な説明】

【図１】本発明による堆積膜表面処理方法を実施するのに用いられるプラズマエッチング装置の構成の概要を示す断面図である。

【図２】図１に図示されたプラズマエッチング装置を用い、半導体素子のシリコン堆積膜をプラズマエッチング加工してｎ型ゲート電極パターンを得る際に、ｎ型ゲー

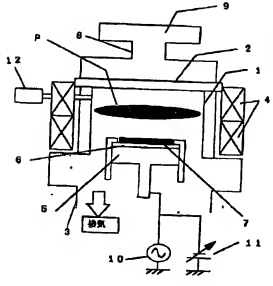
ト電極パターンの変化状態を示す断面図である。

【図3】n型多結晶シリコン部分を既知の表面処理方法によってフラズマエッチング加工し、n型ゲート電極パターンを得る際に、n型ゲート電極パターンの変化状態を示す断面図である。

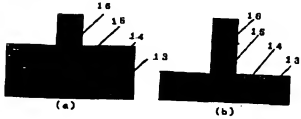
【符号の説明】

1 真空容器
2 マイクロ波導入窓
3 ガス排気口
4 電磁石
5 試料台
6 絶縁膜
7 半導体素子基板（試料）
8 マイクロ波導入部
9 マイクロ波発生源
10 高周波（RF）バイアス電源
12 ガス導入部
13 シリコン基板
14 ゲート酸化膜
15 n型多結晶シリコン部（n型ゲート電極パターン）
16 マスク

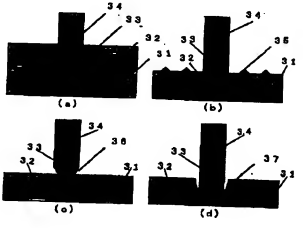
【図1】



【図2】



【図3】



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CLAIMS

[Claim(s)]
[Claim 1] It is the deposition film surface treatment approach which carries out processing processing of the silicon deposition film with a plasma etching system. Divide said processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in said two or more steps is performed. The deposition film surface treatment approach characterized by performing plasma-etching processing using the mixed gas of chlorine (Cl2) and oxygen (O2) in at least one step of the second half in said two or more steps.
[Claim 2] Said silicon deposition film is the deposition film surface treatment approach according to claim 1 characterized by being the thing of JUARU gate membrane structure which shares the film with which conductivity differs.
[Claim 3] Said silicon deposition film is the deposition film surface treatment approach given in either of claims 1 or 2 characterized by being what has the silicide of a refractory metal or a refractory metal.
[Claim 4] The mixed gas of said chlorine (Cl2) and oxygen (O2) is the deposition film surface treatment approach according to claim 1 to 3 characterized by being within the limits whose mixing percentage of oxygen (O2) is 0.5% thru/or 30%.
[Claim 5] Said silicon deposition film is the deposition film surface treatment approach according to claim 1 to 4 characterized by using what uses carbon as a principal component, the thing which consists of silicon nitride, the thing which consists of silicon oxide, or the thing which made these the multilayer as an ingredient of the mask used in case processing processing is carried out.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the deposition film surface treatment approach of having been suitable for performing etching processing of the silicon deposition film on the front face of a semiconductor device especially using a plasma generator, with respect to the deposition film surface treatment approach.
[0002]
[Description of the Prior Art] Conventionally, in the production process of a semiconductor device, down stream processing which carries out etching processing of the silicon deposition film deposited on the processing processing on the front face of a semiconductor device, for example, the front face of a semiconductor device, is included. And usually the plasma etching system is used, the semiconductor device which should carry out etching processing is put in in a plasma etching system, and necessary etching processing is carried out to etching processing of this silicon deposition film in the plasma ambient atmosphere.
[0003] In this case, the plasma etching system indicated by the U.S. Pat. No. 4,490,209 specification is known as what mainly acquires high process tolerance to the plasma etching system used for the etching processing on the front face of a semiconductor device. The plasma etching system indicated here is what added the hydrogen bromide (HBr) in the gas used as the plasma, and can carry out etching processing of the silicon (Si) film which is the quality of a workpiece by having added the hydrogen bromide (HBr) at an anisotropy.
[0004] By the way, the configuration of the semiconductor device which processes such high density information in recent years in connection with various kinds of contents of information having carried out densification is also the thing of the fine structure, and also about the large-scale integrated circuit (LSI) formed in a semiconductor device, in case wiring and an electrode are processed, high process tolerance is required.
[0005] In the semiconductor device of such the fine structure, to constitute the memory device exceeding 256MBit(s), it is necessary to form in 6nm or less the thickness of the gate oxide of each MOS transistor it is thin to the component of a memory device. And since such an MOS transistor becomes the relation of a trade-off of the selection ratio of an anisotropy and the gate oxide of a substrate, obtaining by etching processing is becoming very difficult.
[0006] It can come, simultaneously improvement in the speed and low-power-ization follow on being requested in a semiconductor device in recent years, and many CMOS devices which combined nMOS components, such as a nMOS transistor, and pMOS components, such as a pMOS transistor, are used. This CMOS device dopes p mold impurity in the polycrystalline silicon used as the gate electrode field by the side of pMOS, and is equipped with the so-called JUARU gate structure which doped n mold impurity in the polycrystalline silicon which serves as a gate electrode field in the nMOS side.
[0007]
[Problem(s) to be Solved by the Invention] when it has the complementary gate electrode with which the

gate electrode which differs in conductivity, i.e., p mold gate electrode, and n mold gate electrode were intermingled like a CMOS device, in case the complementary gate electrode section is formed by etching, constraint of processing top versatility will arise so that a single conductive gate electrode section may be described below compared with the case where 4s ** are formed in etching.

[0008] That is, if a lithography process is increased and p mold gate electrode field and n mold gate electrode field are formed by etching processing according to individual when forming a complementary gate electrode for example, the part down stream processing will increase and the whole manufacturing cost will come to increase. For this reason, it is surely necessary to form p mold gate electrode field and n mold gate electrode field by coincidence etching processing. On the other hand, if p mold gate electrode field and n mold gate electrode field are formed by coincidence etching processing It compares with the etch rate of p mold polycrystalline silicon part from which the etch rate of n mold polycrystalline silicon part used as n mold gate electrode serves as p mold gate electrode. Since it is large, The substrate gate oxide near the n mold gate electrode field comes to be early exposed. Etching processing of the exposed gate oxide is carried out, the gate oxide of the processing part may become thin, or it may poke to the gate oxide of the processing part, an omission may arise, and side etch may occur in n mold gate electrode by which etching processing was carried out.

[0009] Drawing 3 (a) thru/or (d) carry out plasma-etching processing of the n mold polycrystalline silicon part by the known surface-preparation approach. In case n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and the condition before processing, (b), or (d) of (a) is in the various conditions after processing. In it The condition that (b) has an etch residue on gate oxide, and (c) show the condition that poked the condition containing side etch, and (d) to n mold gate electrode pattern at gate oxide, and the omission arose.

[0010] For n mold polycrystalline silicon section in which a silicon substrate and 32 doped gate oxide and, as for 33, 31 doped n mold impurity, and 34, as for an etch residue and 36, in drawing 3 (a) thru/or (d), a mask and 35 are [side etch and 37] the gate oxide thrust omission sections.

[0011] First, as the condition before plasma-etching processing is shown in drawing 3 (a), gate oxide 32 is formed in the whole surface of a silicon substrate 31, and n mold polycrystalline silicon section 33 is formed on gate oxide 32. Moreover, n mold gate electrode pattern formation section on n mold polycrystalline silicon section 33 is equipped with the mask 34.

[0012] In the known surface-preparation approach, in case plasma-etching processing is performed, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2) is used. In this case, as etching conditions 0.2 thru/or 4.0Pa, and microwave power by 400 thru/or 1000W [an etching total quantity of gas flow] [50 thru/or 300 mL/min, and the processing pressure force] By choosing the gas mixture ratio of the mixed gas, and the power value of high frequency bias, respectively, it has set up so that suitable plasma-etching processing may be performed.

[0013] However, even if it sets up such etching conditions, it will be in various processing conditions which are described below in many cases.

[0014] As the 1st is shown in the drawing 3 (b), although etching removal of the n mold polycrystalline silicon section 33 of most except n mold gate electrode pattern (n mold polycrystalline silicon section 33) which is in the processing condition which has an etch residue on gate oxide 32, and corresponds to the wearing field of a mask 34 is carried out, the etch residue 35 of n mold polycrystalline silicon section 33 by which etching removal is not slightly carried out on gate oxide 32 remains.

[0015] The 2nd is in the processing condition in which side etch 36 went into processed n mold gate electrode pattern, as shown in the drawing 3 (c). Although etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is carried out Since protection of the side attachment wall of n mold gate electrode pattern is inadequate, etching removal of the n mold gate electrode pattern near a junction field with gate oxide 32 is carried out, and side etch 36 is formed.

[0016] The 3rd is in the processing condition that ran in gate oxide 32 and the section 37 was formed, as shown in the drawing 3 (d). Etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field

of a mask 34 is not only carried out, but Since exposure of the gate oxide 32 of n mold gate electrode pattern circumference was early, sequential etching removal of the exposed gate oxide 32 will be carried out, it runs in gate oxide 32, and the section 37 is formed.

[0017] Thus, unless the etching conditions when performing plasma-etching processing were set up strictly, it was difficult for the known surface-preparation approach to perform processing processing by necessary high process tolerance.

[0018] Then, in etching of a gate electrode pattern, when the gate oxide of a substrate is exposed, it replaces with the process at the time of etching, for example, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2), and a means to prevent the thrust omission of residue, side etch, or gate oxide is provided by carrying out over etching using the mixed gas of a hydrogen bromide (HBr) and oxygen (O2). Over etching processing is performed using [the flow rate of mixed gas] 0.4 thru/or 1.0kW, and bias power as 30 thru/or 40W for microwave power in this case using 100/5 (ml/min) and the processing pressure force as 1.2Pa or more.

[0019] However, this means had the problem that the processing pressure force of processing by the mixed gas of a hydrogen bromide (HBr) and oxygen (O2) was high, and adhesion of the depository object to the processing interior of a room increased.

[0020] In case this invention was made in view of such a technological background and the purpose carries out processing processing of the silicon deposition film with a plasma generator, it is in offering the deposition film surface treatment approach which made it possible to be an anisotropy and to carry out processing processing of the silicon deposition film with high process tolerance.

[0021]

[Means for Solving the Problem] In order to attain said purpose, the deposition film surface treatment approach by this invention It is what carries out processing processing of the silicon deposition film with a plasma etching system. Divide processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in two or more steps is performed. A means to perform plasma-etching processing using the mixed gas of chlorine (Cl2) and oxygen (O2) in at least one step of the second half in two or more steps is provided.

[0022] Until the gate oxide of the substrate of the silicon deposition film is exposed according to said means 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl2) and oxygen (O2)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and n mold gate electrode pattern which side etch does not generate can be formed.

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0024] Drawing 1 is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.

[0025] As shown in drawing 1 , a plasma etching system A vacuum housing 1 and the microwave installation aperture 2 which closes end side opening of a vacuum housing 1, The flueing opening 3 arranged at the other end side of a vacuum housing 1, and the electromagnet 4 installed along with the peripheral face of a vacuum housing 1, The sample base 5 where it has been arranged inside a vacuum housing 1, and the insulator layer 6 was formed in the front face, The semiconductor device substrate 7 used as the sample laid on the sample base 5, and the microwave induction 8 in which the end is carrying out termination by the microwave installation aperture 2, It consists of the microwave generation source 9 connected to the other end of the microwave induction 8, the high frequency (RF)

bias power supply 10 and adjustable DC power supply 11 which were connected conductively to the sample base 5, and gas induction 12 to which gas is introduced in a vacuum housing 1. Moreover, the plasma field P is formed in the interior of a vacuum housing 1.

[0026] In this case, as for the microwave installation aperture 2, the quality of the material consists of transparency matter of microwave (electromagnetic wave), such as a quartz and a ceramic. The microwave outputted from the microwave generation source 9 passes along the microwave induction 8, penetrates the microwave installation aperture 2, and is introduced into the interior of a vacuum housing 1. The gas induction 12 introduces etching gas, such as halogen gas, into the interior of a vacuum housing 1. Inside a vacuum housing 1, microwave acts on this etching gas and the plasma field P by etching gas is formed. An electromagnet 4 generates a magnetic field in a vacuum housing 1. The magnetic field strength in the vacuum housing 1 which an electromagnet 4 generates is chosen so that it is set as the microwave frequency introduced in the vacuum housing 1, and a value which causes resonance, for example, magnetic field strength may turn into about 0.0875T, when a microwave frequency is 2.45GHz. By being chosen as such magnetic field strength, cyclotron movement of the electron in the plasma field P resonates with a microwave frequency, microwave energy is efficiently supplied to Plasma P, and the plasma P of high density is formed.

[0027] Etching processing of the silicon deposition film is carried out, and the semiconductor device substrate 7 is laid on the sample base 5. In this sample base 5, the insulator layer 6 which consists of a ceramic or polymer film is formed in the front face. The high frequency bias power supply 10 supplies high frequency bias to the sample base 5, and the ion which carries out incidence to the semiconductor device substrate 7 is accelerated. Moreover, adjustable DC power supply 11 give direct current voltage to the sample base 5, and make the semiconductor device substrate 7 hold on the sample base 5 according to the electrostatic force then generated.

[0028] Here, the actuation in the case of carrying out etching processing of the silicon deposition film of the semiconductor device substrate 7 is explained to drawing 1 using the plasma etching system of illustration. In this case, the silicon deposition film is n mold polycrystalline silicon which doped and formed n mold impurity in polycrystalline silicon, carries out etching processing of this n mold polycrystalline silicon, and obtains n mold gate electrode pattern.

[0029] In case drawing 2 (a) and (b) carry out plasma-etching processing of the silicon deposition film of the semiconductor device substrate 7 using the plasma etching system illustrated by drawing 1 and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and (a) is in the condition before processing and (b) is in the condition after processing.

[0030] In drawing 2 (a) and (b), n mold polycrystalline silicon section and n mold gate electrode pattern with which a silicon substrate and 14 doped gate oxide and, as for 15, 13 doped n mold impurity, and 16 are masks.

[0031] And as the condition before plasma-etching processing is shown in drawing 2 (a), gate oxide 14 is formed in the whole surface of a silicon substrate 13, and n mold polycrystalline silicon section 15 is formed on gate oxide 14. Moreover, it is the thing of the same configuration as the configuration which n mold gate electrode pattern formation section on n mold polycrystalline silicon section 15 is equipped with the mask 16, and was illustrated by drawing 3 (a).

[0032] By the way, in the deposition film surface-preparation approach by this invention, in case plasma-etching processing to the silicon deposition film of the semiconductor device substrate 7 is performed, necessary plasma-etching processing is performed through two or more steps, and it is divided into the 1st plasma-etching processing until gate oxide 14 is exposed with plasma-etching processing, and the 2nd plasma-etching processing after gate oxide 14 is exposed.

[0033] The 1st plasma-etching processing In this case, hydrogen bromide (HBr) gas, Or it is plasma-etching processing using the mixed gas containing a hydrogen bromide (HBr). In this case, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2) is used. For example, this 1st plasma-etching processing is performed until it sets 0.2-1.0Pa and microwave power to 0.4-1.0kW, it sets bias power to 30W for 70/30/3-5 (ml/min) and the processing pressure force and the great portion of

gate oxide 14 exposes a flow rate. When 1st plasma-etching processing is performed, halogen atom ion and radicals, such as a bromine (Br) and chlorine (Cl2), react with n mold polycrystalline silicon 15, etching processing advances, and, as for the field where it is not equipped with the mask 16 of n mold polycrystalline silicon section 15, n mold gate electrode pattern 15 is formed as a result of the processing. Although most resultants generated at the time of the 1st plasma-etching processing are exhausted, some resultants stick to the side attachment wall of n mold gate electrode pattern 15. In addition, in the 1st plasma-etching processing, the amount of adsorption of the resultant with which the hydrogen (H2) atom contained in a hydrogen bromide (HBr) sticks to the side attachment wall of n mold gate electrode pattern 15 is controlled. For this reason, since side etch may arise to n mold gate electrode pattern 15 although the etching workability of the perpendicular approach improves when mixing percentage of hydrogen bromide (HBr) gas is made high, it may be desirable to choose the mixing percentage of hydrogen bromide (HBr) gas suitably.

[0034] Moreover, the 2nd plasma-etching processing is the plasma-etching processing which used the mixed gas of chlorine (Cl2) and oxygen (O2), for example, it performs this 2nd plasma-etching processing until it sets 90/10 (ml/min) and the processing pressure force to 0.3-1.0Pa, it sets 0.4-1.0kW and bias wave power to 15W for microwave power and an etch residue is lost on gate oxide 14 in a flow rate. Since many of generated resultants stick to the side attachment wall of n mold gate electrode pattern 15 when 2nd plasma-etching processing is performed, although the processing dimension of n mold gate electrode pattern 15 becomes large slightly, side etch does not arise to n mold gate electrode pattern 15, moreover, it runs in the gate oxide 14 of a substrate, the section is not formed in the case of removal of an etch residue, and processing of an anisotropy is attained.

[0035] Consequently, as shown in drawing 2 (b), side etch does not arise to n mold gate electrode pattern 15, but it runs through the condition after plasma-etching processing in the gate oxide 14 of a substrate, and it will be [there is no etch residue on the gate oxide 14 of a substrate,] in the condition that the section is not formed, either, and will become processible [an anisotropy].

[0036] As for the mixed gas of the chlorine (Cl2) used for this 2nd plasma-etching processing, and oxygen (O2), it is desirable to choose it as within the limits whose mixing percentage of oxygen (O2) is 0.5% thru/or 30%.

[0037] On the other hand, although the component of a mask 16 does not contain the thing which uses carbon as a principal component, or carbon, even if it uses any, the same mask function can be demonstrated, but when what does not contain the carbon which consists of silicon nitride, silicon oxide, etc. is used, selectivity with the gate oxide 14 of a substrate becomes high.

[0038] In addition, although the silicon deposition film of the semiconductor device substrate 7 which carries out plasma-etching processing by the deposition film surface-preparation approach by this invention was the example which is the monolayer of n mold polycrystalline silicon section 15 in the aforementioned explanation The silicon deposition film set as the object of the deposition film surface treatment approach by this invention What is JUARU gate membrane structure when p mold dope field where it was not restricted to the example which is the monolayer of n mold polycrystalline silicon section 15, but the deposition film doped p mold impurity, and n mold dope field which doped n mold impurity are shared, On the silicon film, a tungsten (W), nickel (nickel), cobalt (Co), What carried out the laminating of refractory metal layers, such as titanium (Ti), molybdenum (Mo), and chromium (Cr), and the layer which contains the nitride of these metals as barrier film which prevents diffusion, Or even if it is the silicon film which has the silicide of these metals, it is possible to perform plasma-etching processing similarly.

[0039] Moreover, there is no deposition film surface treatment approach by this invention, and it can make the same function attain with respect to the plasma production approach.

[0040] According to the gestalt of the above operation, it replaces with the over etching processing by the mixed gas of the high hydrogen bromide (HBr) and oxygen (O2) of the processing pressure force currently performed conventionally. By performing over etching processing by the mixed gas of the low chlorine (Cl2) of the processing pressure force, and oxygen (O2) the gate oxide of residue, side etch, and a substrate -- also running -- while there is nothing and being able to perform etching processing

processing of high process tolerance in an anisotropy, adhesion of the depository object to a processing room can be lessened.

[0041]

[Effect of the Invention] As mentioned above, until the gate oxide of the substrate of the silicon deposition film is exposed according to the deposition film surface treatment approach of this invention 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl2) and oxygen (O2)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and it is effective in the ability to form n mold gate electrode pattern which side etch does not generate.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the deposition film surface treatment approach of having been suitable for performing etching processing of the silicon deposition film on the front face of a semiconductor device especially using a plasma generator, with respect to the deposition film surface treatment approach.

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PRIOR ART

[Description of the Prior Art] Conventionally, in the production process of a semiconductor device, down stream processing which carries out etching processing of the silicon deposition film deposited on the processing processing on the front face of a semiconductor device, for example, the front face of a semiconductor device, is included. And usually the plasma etching system is used, the semiconductor device which should carry out etching processing is put in in a plasma etching system, and necessary etching processing is carried out to etching processing of this silicon deposition film in the plasma ambient atmosphere.

[0003] In this case, the plasma etching system indicated by the U.S. Pat. No. 4,490,209 specification is known as what mainly acquires high process tolerance to the plasma etching system used for the etching processing on the front face of a semiconductor device. The plasma etching system indicated here is what added the hydrogen bromide (HBr) in the gas used as the plasma, and can carry out etching processing of the silicon (Si) film which is the quality of a workpiece by having added the hydrogen bromide (HBr) at an anisotropy.

[0004] By the way, the configuration of the semiconductor device which processes such high density information in recent years in connection with various kinds of contents of information having carried out densification is also the thing of the fine structure, and also about the large-scale integrated circuit (LSI) formed in a semiconductor device, in case wiring and an electrode are processed, high process tolerance is required.

[0005] In the semiconductor device of such the fine structure, to constitute the memory device exceeding 256MBit(s), it is necessary to form in 6nm or less the thickness of the gate oxide of each MOS transistor it is thin to the component of a memory device. And since such an MOS transistor becomes the relation of a trade-off of the selection ratio of an anisotropy and the gate oxide of a substrate, obtaining by etching processing is becoming very difficult.

[0006] It can come, simultaneously improvement in the speed and low-power-ization follow on being requested in a semiconductor device in recent years, and many CMOS devices which combined nMOS components, such as a nMOS transistor, and pMOS components, such as a pMOS transistor, are used. This CMOS device dopes p mold impurity in the polycrystalline silicon used as the gate electrode field by the side of pMOS, and is equipped with the so-called JUARU gate structure which doped n mold impurity in the polycrystalline silicon which serves as a gate electrode field in the nMOS side.

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, until the gate oxide of the substrate of the silicon deposition film is exposed according to the deposition film surface treatment approach of this invention 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl2) and oxygen (O2)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and it is effective in the ability to form n mold gate electrode pattern which side etch does not generate.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] when it has the complementary gate electrode with which the gate electrode which differs in conductivity, i.e., p mold gate electrode, and n mold gate electrode were intermingled like a CMOS device, in case the complementary gate electrode section is formed by etching, constraint of processing top versatility will arise so that a single conductive gate electrode section may be described below compared with the case where 4s ** are formed in etching.
[0008] That is, if a lithography process is increased and p mold gate electrode field and n mold gate electrode field are formed by etching processing according to individual when forming a complementary gate electrode for example, the part down stream processing will increase and the whole manufacturing cost will come to increase. For this reason, it is surely necessary to form p mold gate electrode field and n mold gate electrode field by coincidence etching processing. On the other hand, if p mold gate electrode field and n mold gate electrode field are formed by coincidence etching processing It compares with the etch rate of p mold polycrystalline silicon part from which the etch rate of n mold polycrystalline silicon part used as n mold gate electrode serves as p mold gate electrode. Since it is large, The substrate gate oxide near the n mold gate electrode field comes to be early exposed. Etching processing of the exposed gate oxide is carried out, the gate oxide of the processing part may become thin, or it may poke to the gate oxide of the processing part, an omission may arise, and side etch may occur in n mold gate electrode by which etching processing was carried out.
[0009] Drawing 3 (a) thru/or (d) carry out plasma-etching processing of the n mold polycrystalline silicon part by the known surface-preparation approach. In case n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and the condition before processing, (b), or (d) of (a) is in the various conditions after processing. In it The condition that (b) has an etch residue on gate oxide, and (c) show the condition that poked the condition containing side etch, and (d) to n mold gate electrode pattern at gate oxide, and the omission arose.
[0010] For n mold polycrystalline silicon section in which a silicon substrate and 32 doped gate oxide and, as for 33, 31 doped n mold impurity, and 34, as for an etch residue and 36, in drawing 3 (a) thru/or (d), a mask and 35 are [side etch and 37] the gate oxide thrust omission sections.
[0011] First, as the condition before plasma-etching processing is shown in drawing 3 (a), gate oxide 32 is formed in the whole surface of a silicon substrate 31, and n mold polycrystalline silicon section 33 is formed on gate oxide 32. Moreover, n mold gate electrode pattern formation section on n mold polycrystalline silicon section 33 is equipped with the mask 34.
[0012] In the known surface-preparation approach, in case plasma-etching processing is performed, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2) is used. In this case, as etching conditions 0.2 thru/or 4.0Pa, and microwave power by 400 thru/or 1000W [an etching total quantity of gas flow] [50 thru/or 300 mL/min, and the processing pressure force] By choosing the gas mixture ratio of the mixed gas, and the power value of high frequency bias, respectively, it has set up so that suitable plasma-etching processing may be performed.
[0013] However, even if it sets up such etching conditions, it will be in various processing conditions which are described below in many cases.

[0014] As the 1st is shown in the drawing 3 (b), although etching removal of the n mold polycrystalline silicon section 33 of most except n mold gate electrode pattern (n mold polycrystalline silicon section 33) which is in the processing condition which has an etch residue on gate oxide 32, and corresponds to the wearing field of a mask 34 is carried out, the etch residue 35 of n mold polycrystalline silicon section 33 by which etching removal is not slightly carried out on gate oxide 32 remains.
[0015] The 2nd is in the processing condition in which side etch 36 went into processed n mold gate electrode pattern, as shown in the drawing 3 (c). Although etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is carried out Since protection of the side attachment wall of n mold gate electrode pattern is inadequate, etching removal of the n mold gate electrode pattern near a junction field with gate oxide 32 is carried out, and side etch 36 is formed.
[0016] The 3rd is in the processing condition that ran in gate oxide 32 and the section 37 was formed, as shown in the drawing 3 (d). Etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is not only carried out, but Since exposure of the gate oxide 32 of n mold gate electrode pattern circumference was early, sequential etching removal of the exposed gate oxide 32 will be carried out, it runs in gate oxide 32, and the section 37 is formed.
[0017] Thus, unless the etching conditions when performing plasma-etching processing were set up strictly, it was difficult for the known surface-preparation approach to perform processing processing by necessary high process tolerance.
[0018] Then, in etching of a gate electrode pattern, when the gate oxide of a substrate is exposed, it replaces with the process at the time of etching, for example, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2), and a means to prevent the thrust omission of residue, side etch, or gate oxide is provided by carrying out over etching using the mixed gas of a hydrogen bromide (HBr) and oxygen (O2). Over etching processing is performed using [the flow rate of mixed gas] 0.4 thru/or 1.0kW, and bias power as 30 thru/or 40W for microwave power in this case using 100/5 (ml/min) and the processing pressure force as 1.2Pa or more.
[0019] However, this means had the problem that the processing pressure force of processing by the mixed gas of a hydrogen bromide (HBr) and oxygen (O2) was high, and adhesion of the depository object to the processing interior of a room increased.
[0020] In case this invention was made in view of such a technological background and the purpose carries out processing processing of the silicon deposition film with a plasma generator, it is in offering the deposition film surface treatment approach which made it possible to be an anisotropy and to carry out processing processing of the silicon deposition film with high process tolerance.

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MEANS

[Means for Solving the Problem] In order to attain said purpose, the deposition film surface treatment approach by this invention It is what carries out processing processing of the silicon deposition film with a plasma etching system. Divide processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in two or more steps is performed. A means to perform plasma-etching processing using the mixed gas of chlorine (Cl2) and oxygen (O2) in at least one step of the second half in two or more steps is provided.
[0022] Until the gate oxide of the substrate of the silicon deposition film is exposed according to said means 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl2) and oxygen (O2)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and n mold gate electrode pattern which side etch does not generate can be formed.
[0023]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.
[0024] Drawing 1 is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.
[0025] As shown in drawing 1 , a plasma etching system A vacuum housing 1 and the microwave installation aperture 2 which closes end side opening of a vacuum housing 1, The flueing opening 3 arranged at the other end side of a vacuum housing 1, and the electromagnet 4 installed along with the peripheral face of a vacuum housing 1, The sample base 5 where it has been arranged inside a vacuum housing 1, and the insulator layer 6 was formed in the front face, The semiconductor device substrate 7 used as the sample laid on the sample base 5, and the microwave induction 8 in which the end is carrying out termination by the microwave installation aperture 2, It consists of the microwave generation source 9 connected to the other end of the microwave induction 8, the high frequency (RF) bias power supply 10 and adjustable DC power supply 11 which were connected conductively to the sample base 5, and gas induction 12 to which gas is introduced in a vacuum housing 1. Moreover, the plasma field P is formed in the interior of a vacuum housing 1.
[0026] In this case, as for the microwave installation aperture 2, the quality of the material consists of transparency matter of microwave (electromagnetic wave), such as a quartz and a ceramic. The microwave outputted from the microwave generation source 9 passes along the microwave induction 8, penetrates the microwave installation aperture 2, and is introduced into the interior of a vacuum housing 1. The gas induction 12 introduces etching gas, such as halogen gas, into the interior of a vacuum

housing 1. Inside a vacuum housing 1, microwave acts on this etching gas and the plasma field P by etching gas is formed. An electromagnet 4 generates a magnetic field in a vacuum housing 1. The magnetic field strength in the vacuum housing 1 which an electromagnet 4 generates is chosen so that it is set as the microwave frequency introduced in the vacuum housing 1, and a value which causes resonance, for example, magnetic field strength may turn into about 0.0875T, when a microwave frequency is 2.45GHz. By being chosen as such magnetic field strength, cyclotron movement of the electron in the plasma field P resonates with a microwave frequency, microwave energy is efficiently supplied to Plasma P, and the plasma P of high density is formed.

[0027] Etching processing of the silicon deposition film is carried out, and the semiconductor device substrate 7 is laid on the sample base 5. In this sample base 5, the insulator layer 6 which consists of a ceramic or polymer film is formed in the front face. The high frequency bias power supply 10 supplies high frequency bias to the sample base 5, and the ion which carries out incidence to the semiconductor device substrate 7 is accelerated. Moreover, adjustable DC power supply 11 give direct current voltage to the sample base 5, and make the semiconductor device substrate 7 hold on the sample base 5 according to the electrostatic force then generated.

[0028] Here, the actuation in the case of carrying out etching processing of the silicon deposition film of the semiconductor device substrate 7 is explained to drawing 1 using the plasma etching system of illustration. In this case, the silicon deposition film is n mold polycrystalline silicon which doped and formed n mold impurity in polycrystalline silicon, carries out etching processing of this n mold polycrystalline silicon, and obtains n mold gate electrode pattern.

[0029] In case drawing 2 (a) and (b) carry out plasma-etching processing of the silicon deposition film of the semiconductor device substrate 7 using the plasma etching system illustrated by drawing 1 and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and (a) is in the condition before processing and (b) is in the condition after processing.

[0030] In drawing 2 (a) and (b), n mold polycrystalline silicon section and n mold gate electrode pattern with which a silicon substrate and 14 doped gate oxide and, as for 15, 13 doped n mold impurity, and 16 are masks.

[0031] And as the condition before plasma-etching processing is shown in drawing 2 (a), gate oxide 14 is formed in the whole surface of a silicon substrate 13, and n mold polycrystalline silicon section 15 is formed on gate oxide 14. Moreover, it is the thing of the same configuration as the configuration which n mold gate electrode pattern formation section on n mold polycrystalline silicon section 15 is equipped with the mask 16, and was illustrated by drawing 3 (a).

[0032] By the way, in the deposition film surface-preparation approach by this invention, in case plasma-etching processing to the silicon deposition film of the semiconductor device substrate 7 is performed, necessary plasma-etching processing is performed through two or more steps, and it is divided into the 1st plasma-etching processing until gate oxide 14 is exposed with plasma-etching processing, and the 2nd plasma-etching processing after gate oxide 14 is exposed.

[0033] The 1st plasma-etching processing In this case, hydrogen bromide (HBr) gas, Or it is plasma-etching processing using the mixed gas containing a hydrogen bromide (HBr). In this case, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl2), and oxygen (O2) is used. For example, this 1st plasma-etching processing is performed until it sets 0.2-1.0Pa and microwave power to 0.4-1.0kW, it sets bias power to 30W for 70/30/3-5 (ml/min) and the processing pressure force and the great portion of gate oxide 14 exposes a flow rate. When 1st plasma-etching processing is performed, halogen atom ion and radicals, such as a bromine (Br) and chlorine (Cl2), react with n mold polycrystalline silicon 15, etching processing advances, and, as for the field where it is not equipped with the mask 16 of n mold polycrystalline silicon section 15, n mold gate electrode pattern 15 is formed as a result of the processing. Although most resultants generated at the time of the 1st plasma-etching processing are exhausted, some resultants stick to the side attachment wall of n mold gate electrode pattern 15. In addition, in the 1st plasma-etching processing, the amount of adsorption of the resultant with which the hydrogen (H2) atom contained in a hydrogen bromide (HBr) sticks to the side attachment wall of n mold

gate electrode pattern 15 is controlled. For this reason, since side etch may arise to n mold gate electrode pattern 15 although the etching workability of the perpendicular approach improves when mixing percentage of hydrogen bromide (HBr) gas is made high, it may be desirable to choose the mixing percentage of hydrogen bromide (HBr) gas suitably.

[0034] Moreover, the 2nd plasma-etching processing is the plasma-etching processing which used the mixed gas of chlorine (Cl2) and oxygen (O2), for example, it performs this 2nd plasma-etching processing until it sets 90/10 (ml/min) and the processing pressure force to 0.3-1.0Pa, it sets 0.4-1.0kW and bias wave power to 15W for microwave power and an etch residue is lost on gate oxide 14 in a flow rate. Since many of generated resultants stick to the side attachment wall of n mold gate electrode pattern 15 when 2nd plasma-etching processing is performed, although the processing dimension of n mold gate electrode pattern 15 becomes large slightly, side etch does not arise to n mold gate electrode pattern 15, moreover, it runs in the gate oxide 14 of a substrate, the section is not formed in the case of removal of an etch residue, and processing of an anisotropy is attained.

[0035] Consequently, as shown in drawing 2 (b), side etch does not arise to n mold gate electrode pattern 15, but it runs through the condition after plasma-etching processing in the gate oxide 14 of a substrate, and it will be [there is no etch residue on the gate oxide 14 of a substrate,] in the condition that the section is not formed, either, and will become processible [an anisotropy].

[0036] As for the mixed gas of the chlorine (Cl2) used for this 2nd plasma-etching processing, and oxygen (O2), it is desirable to choose it as within the limits whose mixing percentage of oxygen (O2) is 0.5% thru/or 30%.

[0037] On the other hand, although the component of a mask 16 does not contain the thing which uses carbon as a principal component, or carbon, even if it uses any, the same mask function can be demonstrated, but when what does not contain the carbon which consists of silicon nitride, silicon oxide, etc. is used, selectivity with the gate oxide 14 of a substrate becomes high.

[0038] In addition, although the silicon deposition film of the semiconductor device substrate 7 which carries out plasma-etching processing by the deposition film surface-preparation approach by this invention was the example which is the monolayer of n mold polycrystalline silicon section 15 in the aforementioned explanation The silicon deposition film set as the object of the deposition film surface treatment approach by this invention What is JUARU gate membrane structure when p mold dope field where it was not restricted to the example which is the monolayer of n mold polycrystalline silicon section 15, but the deposition film doped p mold impurity, and n mold dope field which doped n mold impurity are shared, On the silicon film, a tungsten (W), nickel (nickel), cobalt (Co), What carried out the laminating of refractory metal layers, such as titanium (Ti), molybdenum (Mo), and chromium (Cr), and the layer which contains the nitride of these metals as barrier film which prevents diffusion, Or even if it is the silicon film which has the silicide of these metals, it is possible to perform plasma-etching processing similarly.

[0039] Moreover, there is no deposition film surface treatment approach by this invention, and it can make the same function attain with respect to the plasma production approach.

[0040] According to the gestalt of the above operation, it replaces with the over etching processing by the mixed gas of the high hydrogen bromide (HBr) and oxygen (O2) of the processing pressure force currently performed conventionally. By performing over etching processing by the mixed gas of the low chlorine (Cl2) of the processing pressure force, and oxygen (O2) the gate oxide of residue, side etch, and a substrate -- also running -- while there is nothing and being able to perform etching processing processing of high process tolerance in an anisotropy, adhesion of the depository object to a processing room can be lessened.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.
[Drawing 2] In case plasma-etching processing of the silicon deposition film of a semiconductor device is carried out and n mold gate electrode pattern is obtained using the plasma etching system illustrated by drawing 1 , it is the sectional view showing the change condition of n mold gate electrode pattern.
[Drawing 3] In case plasma-etching processing of the n mold polycrystalline silicon part is carried out by the known surface-preparation approach and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern.
[Description of Notations]
1 Vacuum Housing
2 Microwave Installation Aperture
3 Flueing Opening
4 Electromagnet
5 Sample Base
6 Insulator Layer
7 Semiconductor Device Substrate (Sample)
8 Microwave Induction
9 Microwave Generation Source
10 High Frequency (RF) Bias Power Supply
12 Gas Induction
13 Silicon Substrate
14 Gate Oxide
15 N Mold Polycrystalline Silicon Section (N Mold Gate Electrode Pattern)
16 Mask

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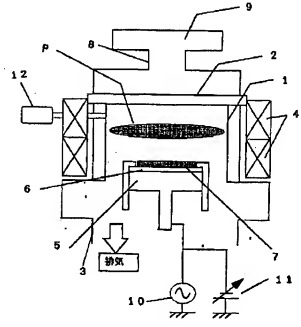
DRAWINGS

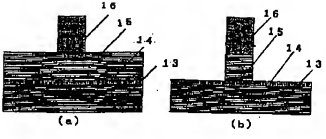
[Drawing 1]

【図１】



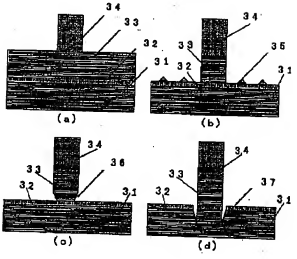
[Drawing 2]

【図２】



[Drawing 3]

【図３】



[Translation done.]